CAPSTONE PROJECT: CMOS Radio-frequency Receiver

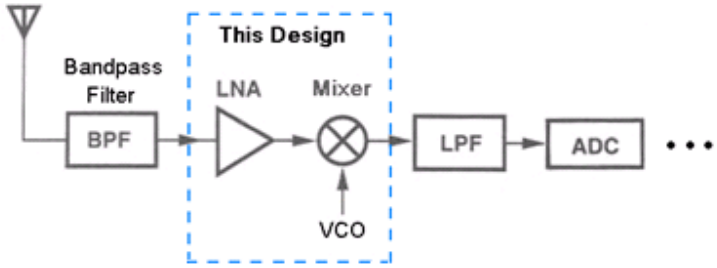

Fig. 1. a typical architecture for a RF receiver

Project Purpose: This design forms a primary part of a RF-frontend of a wireless receiver at the gigahertz band. It may be used in a communication system (e.g. PCS or Europe GSM) or the global positioning system (GPS). The design consists of **a LNA (low noise amplifier) and a mixer and a VCO (or a frequency synthesizer)**. Fig. 1 illustrates a typical architecture of a RF receiver.

The entire project will be designed based on the 0.5-um CMOS process. Depending on the actual performance of this process, the operation frequency may vary from 500MHz to 1.5GHz.

Fig. 2 shows a practical design layout of a 1.5GHz LNA (Shaeffer and Lee).

According to recent research, many narrowband LNAs apply an inductive degeneration (fig. 3) at the source to achieve a perfect impedance match while yielding an attractive noise figure. And a Gilbert cell (fig. 4) is most commonly used for a mixer (either single-end or differential). These schematics might be used as our circuit topology.

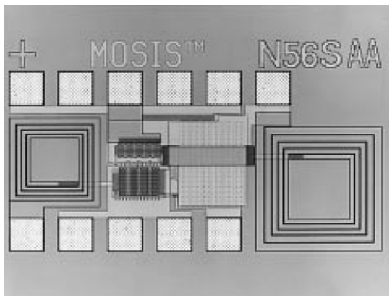

Fig. 2. layout of a 1.5GHz LNA

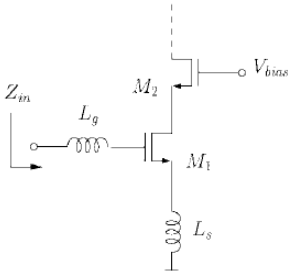

Fig. 3. a cascode L-degen LNA

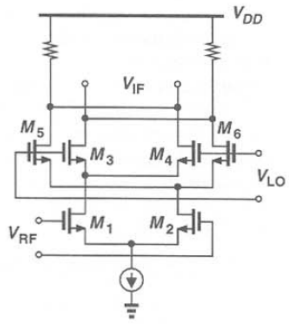

Fig. 4. a Gilbert cell

Project schedule:

- Begin fall 2009
- Project end date – May 2010

Disciplines Needed:

- Analog VLSI
- Microwave engineering, or engineering electromagnetic
- Communication principle and random process

Number of students desired: 3 to 6

Faculty Sponsor: Paul M. Furth

Methodology:

1. Before actually designing the circuit, students need to get familiar with CMOS radio-frequency circuits and analog IC design by reading textbooks.

2. Then, the team will need to solve the following problems:
   - Determine a circuit topology for our design
   - device modeling of the MOSFET (for short-channel device, especially its noise model)
   - Proper usage of SPICE simulator (ADS from Agilent or other equivalent design environment, we will be using BSIM model or Philips MOS9)
   - Transistor layout minimizing the parasitics
   - Modeling of lumped elements (e.g. spiral inductor, Balun) using analytical equation or Electromagnetic solvers (e.g. ADS momentum, Sonnet, IE3D or other equivalents)
   - Modeling of packaging, bond wire and the bond pad
   - ESD protection for a RF circuit(should be different from a conventional ESD)
   - Other critical design considerations such as stability
   - Proper method to simulate/test the parameters of a RF circuits (NF, IP3, etc.)

3. After the computer simulation, we will submit this chip to MOSIS
4. The team will need to design a test board for the IC
5. The last step is to test the performance of our circuits in terms of popular parameters of a RF circuits(Gain, S parameter, IIP3 , NF)
6. The project topology and specifications may be varied according to the actual condition of our design. (e.g. make the LNA of gain variable)

Project deliverables:

1. Analytical analysis of the schematic
2. Software simulation of the circuits (the entire circuits and the spiral inductors)
3. Layout in Cadence (or equivalent software)
4. Prototyped chip from MOSIS

Project Review:

1. Schematic Review
2. Simulation Result Review
3. Experimental Testing review

Outreach Requirements:

A final presentation will be needed.

Make a short video that summarize the project and demonstrate the operation of the design.